DEMODULATION SECTION IN A MULTIPLE PROTOCOL RECEIVER

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The present invention relates to the demodulation and processing of signals modulated according to different modulation schemes, such as satellite signals and terrestrial broadcast high definition signals, for example.

Currently, digital signals carrying programming, such as video/audio/data programming, are transmitted to consumers from different providers in respectively different formats, sometimes referred to as protocols. For example, direct satellite system (DSS) signals are formatted in a proprietary format, and all signals carrying programming supplied via satellites in this system are formatted using that protocol. Similarly, in the United States terrestrial broadcast high definition (HDTV) signals are formatted according to a standard initially proposed by the Advanced Television Standards Committee (ATSC) and approved by the US Federal Communications Committee (FCC), and all terrestrial broadcast HDTV programming signals are formatted using that protocol. In Europe direct video broadcast (DVB) signals may be transmitted by either satellite, or via cable, and all such broadcasts are formatted according to the European standard.

Furthermore, the different digital signals are modulated onto carriers for transmission to consumers using different modulation schemes. For example, the DSS signals are modulated using a quadrature phase shift keyed (QPSK) modulation scheme. The ATSC signals are modulated using a vestigial sideband (VSB) modulation scheme. The DVB satellite signals are modulated using a QPSK modulation scheme, and DVB cable signals are modulated using a quadrature amplitude modulation (QAM) scheme with either a 64 or 256 point constellation. One skilled in the art will further understand that even similar modulation schemes (e.g. QPSK) may use different parameters, such as the excess bandwidth factor, requiring that demodulators for the different QPSK signals be configured differently.

Consumers will want to receive digital signals of any or all of these and any other protocols through which digital signals carrying programming is carried. Currently, this requires separate receivers, each embodied in a separate enclosure, such as a so-called set top box, for each desired protocol. Each such receiver includes a demodulator adapted to the modulation scheme of the modulated digital signal, and a transport processor adapted to the protocol of the demodulated digital signal. However, separate receivers are expensive for the consumer, require a large amount of space for the various set top boxes, and are inconvenient to use. For example, each set top box may have its own remote control that may be incompatible with those of the other set top boxes.

It is, therefore, desirable to provide a single receiver in a single enclosure which can selectively receive any one of multiple protocol digital signals. Such a receiver must include a demodulator section which can selectively demodulate signals modulated by different modulation schemes, and a transport decoder section which can selectively process the demodulated digital signals according to the respectively different protocols.

One prior art solution for such a demodulator section involved analyzing the functions performed by each of the separate demodulators, and providing for a single adaptive demodulator, including function circuits for all the functions required by all the different modulation schemes. Such a demodulator section changes its internal configuration in response to a control signal to provide the functions required to demodulate the currently selected modulation scheme. Because there are some functions which are common to most or all modulation schemes, this technique can provide a practical demodulator which can be reconfigured to demodulate input signals modulated according to any of a plurality of predetermined modulation schemes. U.S. Patents 5,671,253, issued Sept. 23, 1997 to Stewart, and 5,717,471, issued Feb. 10, 1998 to Stewart illustrate such systems.

Such systems include a single adaptive demodulator which can be fabricated on a single integrated circuit (IC) chip and demodulate signals

modulated according to different modulation schemes. For example, U.S. Patent 5,671,253 illustrates a system which can demodulate DSS signals, and DVB satellite and cable signals, and U.S. patent 5,717,471 illustrates a system which can demodulate satellite signals, terrestrial broadcast signals and cable signals. In each of these systems, function circuits are fabricated on the demodulator IC for all of the necessary functions for the desired different modulation schemes with multiplexers between them to reconfigure the circuit in the appropriate manner for each of the modulation schemes desired to be received. Control signals are supplied from a system controller to each of the multiplexers inside the adaptive demodulator to place them in the appropriate state for the desired modulation scheme.

Another prior art solution is to provide separate demodulators for the desired signals, then to provide a multiplexer to connect the desired demodulator to the transport processor in response to a control signal. U.S. Patent application Serial No. 09/427,388 filed Oct. 26, 1999 by Grimes et al. illustrates such a system. In Serial No. 09/427,388 a plurality of demodulators, demodulating signals modulated according to a plurality of modulation schemes, is coupled to a signal multiplexer. Control signals are provided to the multiplexer to condition the multiplexer to connect the desired demodulator to the adaptive transport processor.

In the former prior art solution, it is very expensive to add an additional demodulator. The entire IC chip on which the demodulator section is fabricated must be reanalyzed to determine the new functions required, to design circuitry to provide those new functions and to interconnect that circuitry with the preexisting circuitry. In addition, the control processor for the receiver must provide control signals to all the multiplexers in the IC chip. Adding functionality for an additional demodulator may require additional multiplexers in the IC chip to interconnect the additional function circuits, and/or augmenting existing multiplexers by adding further input terminals. This in turn requires additional control lines for the additional and/or augmented multiplexers. This can require

additional pins on the IC chip, or additional complexity of the system for distributing control signals.

In the latter prior art solution, additional demodulators may be more easily added, but it still requires augmenting the multiplexer connecting those demodulators to the transport processor. This could mean using multiplexer input terminals available but unused. For example, an example of a preexisting multiplexer has four input terminals. In a system originally including three demodulators, a fourth may be added using the fourth available but unused input terminal in such a multiplexer. However, the addition of a fifth demodulator would require a complete redesign of the multiplexer circuit. In either case, addition of demodulators requires additional control signals for that multiplexer and additional pins on the multiplexing chip, or additional complexity in the control signal distribution system.

It is desirable that receivers for signals transmitted in a plurality of protocols, and modulated according to a plurality of corresponding modulation schemes, be constructed so that adding new demodulators is made easy and inexpensive.

In accordance with principles of the present invention, a multiple protocol receiver includes a demodulator section. The demodulator section includes a plurality of demodulators, each demodulator having a tri-state output terminal for generating demodulated digital data. The tri-state output terminals are coupled to a signal bus. The signal bus, in turn, is coupled to a signal processor, such as a transport processor, for processing the demodulated digital data.

A demodulator section designed in such a manner makes it easy to add an additional demodulator. The additional demodulator need only have a tri-state output terminal, as the others do, and be connected to the system bus. No adaptive demodulator need by redesigned, and no multiplexer need by augmented.

In the drawing:

Fig. 1 is a block diagram of a demodulator section of a receiver according to the present invention; and

Fig. 2 is a more detailed block diagram of a demodulator section of a receiver according to the present invention illustrated in Fig. 1.

Fig. 1 is a block diagram of a demodulator section of a receiver according to the present invention. In Fig. 1, a plurality 10 of N demodulators are coupled to respective sources (not shown) of baseband modulated signals, modulated according to one of a plurality of respectively different modulation schemes. Demodulator 1 10(1) demodulates signals according to one modulation scheme (e.g. VSB for HDTV), demodulator 2 10(2) demodulates signals according to a different modulation scheme (e.g. QPSK for DSS). The remainder of the demodulators demodulate signals according to respectively different modulation schemes (e.g. QPSK and QAM for DVB). The respective output terminals of the plurality 10 of demodulators are coupled to a signal bus 20 including data and control signal lines (not shown), in a known manner. The signal bus 20 is also coupled to an input terminal of a transport processor 30. A system controller 40 provides control signals to the plurality 10 of demodulators (and to other circuits - not shown).

Each of the plurality 10 of demodulators includes a tri-state output buffer 12 for coupling signals from the demodulator to the signal bus 20. Each such tri-state output buffer includes a control input terminal OE. The system controller 40 provides a control signal to each of the output enable input terminals of the tri-state buffers 12.

In operation, the system controller 40 provides an output enable control signal to the tri-state buffer 12 of only a selected one of the plurality 10 of demodulators. In response to such a control signal the tri-state buffer 12 in the selected demodulator 10 produces logic level signals representing the demodulated digital data from that demodulator 10. The remainder (i.e. non-selected ones) of the plurality 10 of demodulators receive control signals to

disable the outputs of the tri-state buffer 12. In response to such control signals, the output terminals of the tri-state buffers are conditioned to exhibit a high output impedance.

Consequently, the selected one of the plurality 10 of demodulators is coupled to the signal bus 20, while the other ones of the plurality 10 of demodulators are isolated from the signal bus 20. Signals from the selected one of the plurality 10 of demodulators are, thus, supplied to the transport processor 30 via the signal bus 20. The system controller 40 supplies control signals (not shown) to the transport processor 30, in a known manner. In response, the transport processor 30 processes the demodulated digital signals from the selected one of the plurality 10 of demodulators in the appropriate manner to generate a payload signal (not shown) which is further processed, also in a known manner.

In such a receiver, it is possible to provide as many demodulators as required to demodulate all the desired signal protocols. It is further possible to easily expand the number of demodulators in the receiver to add another protocol. It is neither necessary to redesign a signal adaptive demodulator IC chip, nor is it necessary to augment a multiplexer, as in prior art solutions.

Fig. 2 is a more detailed block diagram of the demodulator section of a receiver according to the present invention illustrated in Fig. 1. In Fig. 2, those elements which are the same as those illustrated in Fig. 1 are designated by the same reference numbers and are not described in detail below. In order to simplify the figure, only two demodulators, 10(1) and 10(2), are illustrated. One skilled in the art will understand that more than two demodulators may be included in a system in accordance with the present invention.

In Fig. 2, each of the plurality 10 of demodulators generates four signals carrying the demodulated digital data from that demodulator. In Fig. 2, the digital data is carried in the form of a serial bit stream. A data signal (DATA) is generated carrying a non-return-to-zero (NRZ) format serial data stream signal

representing the demodulated digital data, and a corresponding clock signal (CLOCK) is generated carrying timing information to permit clocking of that data into following circuitry. For example, for DSS format data, the serial data is produced at substantially 42 MHz, while for HDTV format data, the serial data is produced at substantially 43 MHz. Other formats produce serial data at different data rates. The transport processor 30 is fabricated to be able to process serial data at all of the data rates produced by the plurality 10 of demodulators.

Further signals produced by the plurality 10 of demodulators are a packet valid signal (PACKET VALID), and a packet data signal (PACKET DATA). The packet valid signal (PACKET VALID) is conditioned to assume one logic state when the data in the packet currently being carried on the signal bus 20 is valid and the other logic state when the current packet had so many errors that the data could not be accurately recovered. The packet data signal (PACKET DATA) is conditioned to assume one logic state when the serial data currently being carried on the signal bus 20 represents transport data and the other logic state when the serial data currently being carried by the signal bus 20 represents overhead information, such as error detection and correction code information. The transport processor 30 will ignore packets that are not valid, and serial data that does not represent transport data, as indicated by the PACKET VALID and PACKET DATA signals.

These four signals are generated by each one of the plurality 10 of demodulators in a known manner by circuitry of known design (not shown) and supplied to the respective tri-state buffer circuits 12. Respective output terminals of the tri-state buffer circuits 12 are coupled to corresponding signal lines in the signal bus 20, illustrated in more detail in Fig. 2. One skilled in the art will understand that the signal characteristics, both physical and logical, for these signals must be the same in each one of the plurality 10 of demodulators.

The system controller 40 generates control signals for the plurality 10 of demodulators. A control register 14 in each one of the plurality 10 of demodulators is coupled to receive the control signal from the system controller

40 in a known manner. An output terminal of the control register 14 is coupled in common to the output enable input terminal of the tri-state buffers 12.

One skilled in the art will understand that control signals may be supplied from the system controller 40 to the plurality 10 of demodulators by any of a number of known schemes. For example, the system controller 40 may be implemented with a microprocessor, and each one of the plurality 10 of demodulators may be coupled in common to the control bus of the microprocessor. In a illustrated embodiment, the plurality 10 of demodulators are coupled to and controlled by a microprocessor via a Philips I2C control bus, in a known manner.

The signal bus 20 consists of four signal lines: a first for the serial data signal DATA and a second for the serial data clock signal CLOCK. These two lines comprise the data portion of the signal bus 20. A third signal line is for the packet valid signal (PACKET VALID) and a fourth signal line is for the packet data signal (PACKET DATA). These two signal lines comprise the control portion of the signal bus 20. The transport processor 30 receives these signals, extracts the digital data, and if it the packet is valid, and the current data bits represent transport data, processes the data to extract the payload, all in a known manner.

In Fig. 2, the signal bus 20 is coupled to the transport processor 30 through an optional buffer circuit 25, shown in phantom in Fig. 2. The buffer circuit 25 provides additional drive power for the signals in the signal bus 20. This may be necessary if the plurality 10 of demodulators are not collocated with the transport processor 30. For example, if the plurality 10 of demodulators are on one or more IC chips, and the transport processor is on a different IC chip, then the signal bus must travel through e.g. printed circuit board (PCB) traces. In order to provide relatively robust transmission, the buffer 25 is required.

In addition, in the illustrated embodiment, the plurality 10 of demodulator circuits are fabricated using a 3.3 volt CMOS process, while the transport processor 30 is fabricated using 5 volt TTL process. In this system design, the

buffer circuit 25 also includes specially designed power-on circuitry to keep the output terminals off during power up. This prevents the 3.3 v. CMOS output terminals of the plurality 10 of demodulator IC chips from inadvertently latching the 5 v. input terminals of the transport processor 30 during power up.

In Fig. 2, the signal bus 20 is illustrated as including 4 signal lines. One skilled in the art will understand that other arrangements are possible. For example, the demodulated digital data could be represented in parallel form instead of serial form. In such an arrangement, there would be e.g. eight data lines for a byte of data. The clock signal CLOCK would be a byte clock in this arrangement. This increases the number of pins necessary on the plurality 10 of demodulators and the transport processor 30 (and the buffer 25), and increases the number of tri-state buffers 12 required in each demodulator 10, but decreases the output bit rate of the signal bus 20 by a factor of e.g. eight. It is also possible to eliminate the PACKET DATA signal if additional circuitry in the transport processor 30 is provided to monitor the data stream and determine which of the data bits (or bytes) represents transport data and which represents error detection and correction data. Similarly, it is possible to eliminate the PACKET VALID signal by including an indication of the validity of the data within the packet data itself. It is finally possible to eliminate the data clock signal CLOCK by using a self clocking data signal instead of the NRZ signal of the illustrated embodiment. Thus, a minimum of one output terminal, carrying a self-clocking data signal is possible. It is considered, however, that the illustrated embodiment is the most practical arrangement for the signal bus 20.